PROCESS AND APPARATUS FOR PLACEMENT OF MEGACELLS IN ICs DESIGN

ABSTRACT OF THE DISCLOSURE

An IC layout containing megacells placed in violation of design rules is corrected to remove design rule violations while maintaining the original placement as near as practical. The sizes of at least some of the megacells are inflated. The megacells are placed and moved in a footprint of the circuit in a manner to reduce placement complexity. The placement of the megacells is permuted to reduce placement complexity. Additional movements are be applied to the permuted placement to further reduce placement complexity.